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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,718	06/22/2000	Francis G. Celii	TI-29276	8761

7590 06/04/2003
Jacqueline J Garner
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EXAMINER

MACKEY, TERRENCE M

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/599,718	Applicant(s) CELII ET AL.	
	Examiner Terrence Mackey	Art Unit 1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 3/17/03.
- 2a) ☐ This action is FINAL.
- 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

Detailed Action

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 – 5 and 12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear the relationship by which the selective etching through the shelf layer using the via pattern after said etching a via step may be accomplished prior to the step of extending the via by selectively etching the intrametal dielectric layer which is in overlying relationship thereto.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 – 14 are rejected under 35 USC 103 (a) as being unpatentable over Grill et al. (6,140,226) in view of either Hung et al (6,380,096) or Wang et al. (6,057,239). Applicant claims a process for a process of fabricating an integrated circuit comprising the following steps performed in order: forming an interlevel dielectric layer

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over a semiconductor substrate, forming an intrametal dielectric layer over said interlevel dielectric layer, forming a hardmask over said intrametal dielectric layer, forming a via pattern over said hardmask, selectively etching a via through said hardmask, extending said via by selectively etching said intrametal dielectric layer, depositing a BARC layer over said hardmask and within said via, wherein the BARC is significantly thicker within said via than over said hardmask, forming a trench pattern over said BARC layer, and etching a trench in said intrametal dielectric layer, wherein said etching a trench step further removes at least a portion of said BARC layer within said via and wherein at the conclusion of said etching a trench step said via extends through said interlevel dielectric layer.

Grill et al. illustrate as prior art in Figures 1A – 1L (and the accompanying description on column 3, line 60 through column 5, line 8) a dual damascene process flow comprising steps of forming a layered dielectric stack comprising an optional dielectric passivation/adhesion layer, a via level dielectric, an optional dielectric etch stop layer, and a wiring level dielectric, forming a hardmask layer thereon, forming a via level pattern in the hardmask layer and transferring the via pattern to the wiring level dielectric, forming a wiring level pattern in the hardmask and etching the exposed regions of the layered dielectric stack to transferring the wiring pattern to the entire thickness of the wiring level dielectric while simultaneously transferring the via pattern to the entire thickness of the via level dielectric. The reference teaches the use of organic polymer dielectrics as well as other dielectric materials for the via and wiring dielectric layers (column 4, lines 5-11). Grill et al. do not teach the formation of a BARC layer over the hardmask prior to forming the wiring pattern.

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Hung et al. and Wang et al. teach dual damascene process flows wherein the trench opening is formed subsequent to the via opening. Both references teach the formation of anti-reflective coating material into an opening in a dielectric layer wherein the anti-reflective material is significantly thicker within the opening than over the dielectric layer and subsequently etching the dielectric layer to form an enlarged opening for the wiring level of the dual damascene wiring structure. The use of the anti-reflective coating is disclosed as being particularly useful in dual damascene process flows requiring two photolithographic patterning steps and concomitant etching steps. It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize an anti-reflective layer formed significantly thicker within the via opening than on the hardmask layer as taught by Hung et al. and Wang et al. in the process flow of Grill et al. so as to provide improved control of the photolithographic patterning and etching steps in the formation of a dual damascene wiring structure for an integrated circuit.

Conclusion

Remaining references cited to show the state of the prior art.

No claims are allowed.

Papers relating to this application may be submitted to Technology Sector 1700 by facsimile transmission. Papers should be faxed to Crystal Plaza 3, Art Unit 1765, using fax number (703) 305-6357. All Technology Section 1700 fax machines are available to receive transmissions 24 hrs/day, 7 days/wk. Please note that the faxing of such papers must conform to the Notice published in the Official Gazette, 1096 OG 30, (November 15, 1989).

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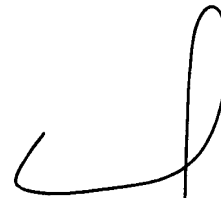
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Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Terrence Mackey whose telephone number is (703) 305-5504. The Examiner can normally be reached Monday - Friday from 7:00 AM – 4:30 PM. Attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, Ben Uteck, can be reached at (703) 308-3836.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0661.

TMM

May 27, 2003

A handwritten signature in black ink, consisting of a stylized 'R' followed by a vertical line and a loop.

ROBERT KUNEMUND
PRIMARY EXAMINER